**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

| | | |
|---|---|---|
| MICROUNITY SYSTEMS ENGINEERING, INC., Plaintiff, | § | CIVIL ACTION NO. 2-04-CV-120 (TJW) |
| v. | § | |
| DELL, INC. and INTEL CORPORATION, Defendants. | § | |

**MEMORANDUM OPINION AND ORDER**

After considering the submissions and the arguments of counsel, the court issues the following order concerning the claim construction issues:

## I. Introduction

In this patent infringement suit, Plaintiff Microunity Systems Engineering, Inc. accuses Defendants Dell, Inc. and Intel Corporation of infringing eight United States patents. U.S. Patent Nos. 5,742,840 ( "the '840 patent"), 5,794,060 ("the '060 patent"), 5,809,321 ("the '321 patent"), 5,794,061 ("the '061 patent"), 6,584,482 ("the '482 patent"), 6,643,765 ("the '765 patent"), and 6,725,356 ("the '356 patent") disclose a method and apparatus for the processing of multi-media digital communications. Collectively, these seven patents are referred to as the "media processor patents."[1] The plaintiff also asserts U.S. Patent No. 5,630,096 ("the '096 patent") against the defendants. The '096 patent discloses "a controller for maximizing throughput of memory requests from an external device to a synchronous DRAM."

The invention disclosed in the '840, '060, '061, and '321 patents generally "relates to the field of communications processing, and more particularly, to a method and apparatus for real-time

[1] The '840, '060, '061, and '321 patents share a common specification. The '765 and '356 patents also share a common specification.

processing of multi-media digital communications." '840 patent, col. 1, ll. 15-17. The '765 and '356 patents relate to general purpose processor architectures, and in particular, wide operand architectures. '765 patent, col. 1, ll. 19-21. These media processor patents disclose microprocessor designs that are capable of processing different types of media data, including audio, video, and graphics data, at very high volume in real-time.

## II. Law Governing Claim Construction

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, the court looks to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. Under the patent law, the specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own

lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). And, although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This court's claim construction decision must be informed by the Federal Circuit's recent decision in *Phillips v. AWH Corporation*, 2005 WL 1620331 (Fed. Cir. July 12, 2005)(en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the *claims* of a patent define the invention to which the patentee is entitled the right to exclude." 2005 WL 1620331, at *4 (emphasis added)(*quoting Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* at *5. The ordinary and customary meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e. as of the effective filing date of the patent application." *Id.* This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention. The patent is addressed to and intended to be read by others skilled in the particular art. *Id.*

The primacy of claim terms notwithstanding, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms,

those terms are part of "a fully integrated written instrument." *Id.* at **6-7 (*quoting Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id.* at **7-8. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims." *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. The prosecution history helps to demonstrate how the inventor and the PTO understood the patent. *Phillips*, 2005 WL 1620331 at *9. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence. That evidence is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims.

*Phillips* rejected any claim construction approach that sacrificed the intrinsic record in favor

of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Id*. at **13-14. The approach suggested by *Texas Digital*–the assignment of a limited role to the specification–was rejected as inconsistent with decisions holding the specification to be the best guide to the meaning of a disputed term. *Id.* According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of the claim terms within the context of the patent." *Id*. at *14. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id*. What is described in the claims flows from the statutory requirement imposed on the patentee to describe and particularly claim what he or she has invented. *Id.* The definitions found in dictionaries, however, often flow from the editors' objective of assembling all of the possible definitions for a word. *Id.*

*Phillips* does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id*. at *16. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant. The court now turns to a description of the technology in the case, followed by an assessment of the terms and phrases in dispute.

## III. Discussion

The parties refer to seven of the patents as the media processor patents. In general, these patents describe an invention designed to consolidate the functions of several separate processors into a single processor for processing multi-media digital communications. As described in the abstract, the inventions relate to a general purpose, programmable media processor for processing and transmitting a media data stream of audio, video, radio, graphics, encryption, authentication, and networking information in real-time. '840 patent, Abstract. In the patents, the inventors noted certain shortcomings of application specific integrated circuits ("ASICs") as a solution to the efficient processing of broadband media data. The solution to using a number of different ASICs was to develop a single unified media processor. By combining the functionality of the various ASICs into a single processor, referred to as a media processor, the patentees sought to avoid the various problems associated with the use of a multiplicity of application-specific circuits.

The media processor incorporates the functionality of the different ASICs into a processor that can process the different media data types having different data sizes. The execution and arithmetic units can process different data types and sizes, at least in part, because of an ability referred to as "dynamic partitioning." The incoming data, which may be of different types, can be divided in accordance with the type of data it is. As the input data type changes (e.g. from video to audio), the data size may change, requiring a different partitioning. Because the execution and arithmetic units can process media data of different types and sizes, there is no time where a substantial amount of silicon "real estate" is idle. Moreover, the media processor is very flexible because the execution and arithmetic units are not limited to operating on any one particular data type, but can accommodate media data of different types and sizes. Finally, to maximize throughput

of the media processor, the execution and arithmetic units can perform operations on a group of data for each instruction, rather than each operation requiring a separate instruction.

In addition to the media processor patents, the plaintiff has asserted the '096 patent against the defendants. The '096 patent describes a memory controller for maximizing throughput of memory requests. The controller provides an interface between the memory and other devices, such as a processor. The controller enables reading data from, and writing data to, the memory by, for example, the processor. The controller can reorder memory requests and/or otherwise sort memory requests to make maximum use of the available opportunities for data transfer.

### A. Disputed Terms of the Media Processor Patents

#### 1. A plurality of media data streams

The first group of disputed claim terms involves the media data streams processed by the processor. The plaintiff contends that "a plurality of media data streams" means "two or more different types of media data streams such as audio, video, radio, graphics, encryption, authentication, and/or network information." The defendants urge that "a plurality of media data streams" means "two or more concurrent streams of audio, video, radio, graphics, encryption, authentication, and/or network media data information from two or more sources." At issue is the defendants' use of the word "concurrent" in their proposed construction. After considering the submissions of counsel and the intrinsic record, the court is persuaded that the plaintiff's position is correct. Accordingly, the court construes "a plurality of media data streams" to mean "two or more different types of media data streams."

#### 2. Unified media data streams

The court construes "unified media data streams" to mean "combined media data streams of

different types."

**3. Unified execution of multiple media data streams**

The plaintiff proposes that "unified execution of multiple media data streams" be construed to mean "processing two or more different types of media data streams by the same execution unit." On the other hand, the defendants submit that the disputed phrase means "operating on two or more media data streams in parallel, all at the same time with the same processor, without external specialized processors." The parties' primary dispute is whether media data streams are processed "in parallel," "all at the same time," and "without external processors." The defendants correctly note that the general purpose media processor claimed in the patents was an improvement over the combination of prior art specialized processors; however, the court does not read the claim language or the specification to exclude all use of external processors. What is required is that the media processor has the capability of processing two or more different types of media data streams by the same execution unit. The court is persuaded that the plaintiff's proposed construction is correct. Accordingly, the court construes "unified execution of multiple media data streams" to mean "processing two or more different types of media data streams by the same execution unit."

**4. Capable of dynamic partitioning**

All of the asserted claims of the media processor patents recite the phrase "dynamic partitioning" or a similar limitation. The plaintiff urges that "capable of dynamic partitioning" means "able to divide the data into separate and distinct operands on an instruction by instruction basis." The defendants contend that the disputed phrase means "capable of dividing width-wise into a variable number of elements for simultaneous parallel processing of any combination or permutation of media data types in any size."

The parties' briefs and their hearing presentation focused on whether the court could (or should) consider an Appendix filed with the PTO in connection with this term. The court has concluded that resort to the Appendix is unnecessary, and that the specification is sufficiently illuminating to permit construction of this term. The specification of the '840 patent shows a Table I. Table I is an illustration of an instruction set for the media processor. That table illustrates data can be partitioned into byte-sized portions. Table I does not show partitioning of data on any basis other than a byte, or 8-bit level, nor does it show an instruction set capable of operating on data divided into different partition widths in the data path for any given 32-bits of data. Although Table I does not necessarily exclude a processor with the capability to partition data to the extent required by the defendants' proposed construction, Table I is more consistent with the plaintiff's proposed definition, as it illustrates precisely the type of dynamic partitioning that the plaintiff's construction permits. After considering the submissions of counsel and the intrinsic record, the court construes "capable of dynamic partitioning" to mean "capable of dividing width-wise into a variable number of elements."

**5. Capable of dynamic partitioning based on the elemental width of data received from the data path, the elemental width being equal to or narrower than the data path**

For the same reasons advanced above, the court construes "capable of dynamic partitioning based on the elemental width of data received from the data path, the elemental width being equal to or narrower than the data path" to mean "capable of dividing width-wise into a variable number of elements no wider than the data path, based upon the size of the data elements received from the data path."

**6. Partitioning first and second registers into a plurality of floating point operands, said floating point operands having a defined bit width, wherein said defined bit width is dynamically variable**

The court construes "partitioning first and second registers into a plurality of floating point operands, said floating point operands having a defined bit width, wherein said defined bit width is dynamically variable" to mean "dividing a first and a second register width-wise into a variable number of floating point operands based upon a variable width of the floating point element."

**7. Dynamically partition data received from the data path to account for an elemental width of the data wherein the elemental width of the data is equal to or narrower than the data path**

The court construes "dynamically partition data received from the data path to account for an elemental width of the data wherein the elemental width of the data is equal to or narrower than the data path" to mean "dividing width-wise into a variable number of elements no wider than the data path, based upon the size of the data elements received from the data path."

**8. Dynamically partitionable arithmetic unit**

The court construes "dynamically partitionable arithmetic unit" to mean "the arithmetic unit can be divided into a variable number of elements."

**9. Unified media processing**

The court now turns to the disputed terms relating to the media processor limitations. The plaintiff urges that "unified media processing," as used in the preamble, is not a limitation. Rather, the plaintiff contends that this is a statement of intended use. The defendants contend, however, that "unified media processing" is a limitation, and means "processing a media data stream using parallel processing and utilizing the entire width of the data path through dynamic portioning, without

external specialized processors."

After considering the submissions of counsel, the court concludes that "unified media processing" is not a claim limitation. The phrase "unified media processing" appears in the preamble of claim 1 of the '321 patent, which provides "[a] system for unified media processing, comprising . . ." '321 patent, claim 1. The rule in the Federal Circuit is that "[i]n general, a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l v. Coolsavings.com*, 289 F.3d 801, 808 (Fed. Cir. 2002). The phrase "unified media processing" does not appear in the body of the claim, is not necessary to give life, meaning and vitality to the claim, and does not provide an antecedent basis for the term "media processor," which does appear in the claim. The court therefore concludes that "unified media processing" is not a claim limitation. No construction of this phrase is necessary.

**10. General purpose media processor/ General purpose programmable media processor/ Media processor/ Programmable media processor/ General purpose [multiple precision parallel operation] programmable media processor**

Next, the court turns to the construction of the media processor terms. The plaintiff contends that the "general purpose media processor" is "a general purpose processor that also does media processing." The defendants urge that "general purpose media processor" means "a single programmable processor that processes multiple media data streams without external specialized processors." There are two disputes between the parties regarding the construction of this term and the remaining "media processor" terms. The primary dispute between the parties is whether the "media processor" operates without "external specialized processors." A second issue is whether the term "programmable media processor" is a claim limitation.

After considering the submissions and arguments of counsel, the court construes each of the disputed phrases above to mean "a processor having an execution unit capable of operating on different media types and data sizes." The court is not persuaded that the claim language or the specification necessarily excludes the presence of other, external processors, from the scope of the claim, as long as the processor itself has the requisite capabilities. With respect to the term "programmable media processor," the court concludes that this term is not a claim limitation for the same reasons provided with respect to the term "unified media processing."

**11. Multi-precision arithmetic unit**

The parties largely agree on the construction of "multi-precision arithmetic unit" with one exception. The plaintiffs contend that the "multi-precision arithmetic unit" is "a unit that can perform addition, subtraction, multiplication, division, and other integer and floating point arithmetic operations on data streams of varying sizes." The defendants object to the plaintiff's proposed construction on two grounds. First, the defendants contend that the term "unit" refers to a defined circuit block, and not circuitry distributed across the media processor, as the plaintiff argues. Second, the defendants further contend that the language "other integer and floating point arithmetic operations" should not be included in the construction. Thus, the defendants propose the following construction of "multi-precision arithmetic unit" – "a unit that can perform addition, subtraction, multiplication, division, and other arithmetic operations on data streams of varying sizes." The '840 patent provides as follows:

> Many of the logic blocks themselves can also replaced [sic] with a single multi-precision arithmetic unit, which can be internally partitioned under software control to perform addition, multiplication, division, and other integer and floating point arithmetic operations on symbol streams of varying widths while sustaining the full data throughput of the memory hierarchy.

'840 patent, col. 2, ll. 58-65. Based on the cited portion of the specification, the court is persuaded that the plaintiff's construction is correct and adopts it. The court declines to further define "unit" to require a single circuit block.

**12. Multi-precision execution unit**

The court construes "multi-precision execution unit" to mean "a unit that receives instructions and executes the instructions to perform simultaneous parallel operations on the plurality of media data streams, each of a width up to the width of the data path."

**13. Operable to perform unique operations on each component symbol**

The plaintiff proposes that "operable to perform unique operations on each component symbol" should be construed to mean "capable of performing a distinct operation on each component of a data unit." The defendants urge that the disputed phrase means "able to simultaneously perform different operations on each partitioned item of data." At issue is the meaning of the term "unique." The plaintiff contends it is sufficient that the multi-precision execution unit performs the same, single chosen type of operation (*e.g.*, multiply) on each component symbol, albeit in different, separate, and distinct instances." *See* Plaintiff's Reply Brief at 33. The defendants insist, however, that the plaintiff's construction should be rejected because it does not reflect the definition of the term "unique." After considering the submissions of counsel, the court concludes that the plaintiff is correct. The court defines this term to mean "operable to perform unique operations on each component symbol" to mean "capable of performing a distinct operation on each component of a data unit."

**14. A switch coupled to the data path and programmable to manipulate data received from the data path, the switch providing data streams to the data path**

The plaintiff asserts that this phrase should be construed to mean the following: "a routing device that is: (1) coupled to and receives data from the data path, (2) rearranges the data fields received from the data path in different ways in response to instructions by performing operations such as deals, shuffles, shifts, expands, compresses, swizzles, permutes, and reverses, and (3) provides the rearranged data fields to the data path." The defendants, however, urge that the disputed phrase should be construed more broadly to "hardware and/or software that performs data handling operations on unified media streams." They argue that the plaintiff's proposed construction imports limitations from the specification by requiring that the switch perform operations such as "deals, shuffles, shifts, expands, compresses, swizzles, permutes, and reverses." In the context of these patents, the court construes "a switch coupled to the data path and programmable to manipulate data received from the data path, the switch providing data streams to the data path" to mean "a routing device that is: (1) coupled to and receives data from the data path, (2) rearranges the data fields received from the data path in different ways in response to instructions, and (3) provides the rearranged data fields to the data path."

**15. Manipulating component fields**

The court construes "manipulating component fields" to mean "rearranging the data fields received from the data path in different ways."

**16. Group data handling operations**

The court construes "group data handling operations" to mean "data handling operations applied to a group of partitioned fields."

**17. Register controllable cross bar switch**

The plaintiff asserts that "register controllable cross bar switch" means "a routing device that

selectively couples a plurality of outputs to a plurality of inputs under the control of the contents of a register." The defendants propose that "register controllable cross bar switch" means "a switch which can independently connect any input to any output, and that is controlled through the use of hardware storage locations in the media processor that are available to the user/programmer." At issue is whether the "cross bar switch" must be able to connect any input with any output.

The plaintiff contends that "switch 104," which is described in the specification of the '061 patent, is the cross-bar switch recited in the claims. According to the plaintiff, the specification does not require that "switch 104" be able to connect any input with any output. The defendants, on the other hand, argue that "cross bar switch" is a term of art that means "a switch that allows any input to be connected to any output." The defendants note that the term "cross bar" does not appear in the specifications of the media processor patents and that there is no indication that the patents use the term "cross bar" in a manner different from its ordinary meaning. After considering the submissions of counsel, the court construes "register controllable cross bar switch" to mean "a routing device that selectively couples a plurality of outputs to a plurality of inputs under the control of the contents of a register."

**18. Extended mathematical element**

The plaintiff proposes that "extended mathematical element" be construed to mean "a unit that performs additional mathematical operations that are specialized operations for efficient media processing." The defendants object to the plaintiff's use of the language "specialized operations for efficient media processing." They also contend that the specification of the '840 patent provides that "operations performed by the extended mathematical unit are 'higher level' than those performed by the ALU . . ." Defendants' Sur-reply Brief at 13. Thus, the defendants urge that

"extended mathematical element" be construed to mean "a unit that performs higher level mathematical operations than the arithmetic unit." After considering the submissions of counsel, the court construes "extended mathematical element" to mean "a unit that performs additional mathematical operations other than addition, subtraction, multiplication, division, and other floating point operations."

**19. An extended mathematical element coupled to the data path and programmable to implement additional mathematical operations at substantially peak data throughput**

The court construes "an extended mathematical element coupled to the data path and programmable to implement additional mathematical operations at substantially peak data throughput" to mean "a programmable unit coupled to the data path that performs additional mathematical operations other than addition, subtraction, multiplication, division, and other floating point operations at substantially peak data throughput."

**20. Table look-up . . . [operation]**

The court construes "table look-up . . . [operation]" to mean "an operation that uses a known value to locate an unknown value in a table."

**21. Storing the unified media data streams in a general register file**

The plaintiff submits that "storing the unified media data streams in a general register file" means "storing the unified media data streams in a set of registers, which may be addressed by their number in the set, in which the registers can be used for various purposes." The defendants assert that the disputed phrase means "storing the unified media data streams in a set of hardware storage locations that are available to the user/programmer for a wide variety of functions." Primarily at issue is whether "a general register file" must be available for a "wide variety" of functions.

The plaintiff contends that the "general register file" need not be available for a wide variety of functions, but must be available for "different" or "various" purposes. The plaintiff asserts that its proposed construction is supported by the specifications of the '060 and '840 patents and that its construction would be understood by one ordinarily skilled in the art. According to the plaintiff, the patent specifications only require that the registers not be dedicated or specific purpose registers. The defendants, on the other hand, contend that the media processor patents use the term "general register file" consistent with its ordinary meaning, which requires that the register file be available for "a wide variety of functions." After considering the submissions of counsel, the court construes "storing the unified media data streams in a general register file" to mean "storing the unified media data streams in a set of hardware storage locations that are available to the user/programmer for various purposes."

**22. Multiple operands in partitioned fields of operand registers**

The court construes "multiple operands in partitioned fields of operand registers" to mean "more than one object upon which operations are performed, each object being stored in a separate and distinct field of a register."

**23. Storing partitioned data in registers**

The plaintiff contends that "storing partitioned data in registers" means "storing in registers the data that was divided into separate and distinct data fields." The defendants, on the other hand, argue that "storing partitioned data in registers" means "the results of the dynamic partitioning of the data stream is [sic] stored in adjacent portions of registers." The plaintiff disagrees with the defendant's proposed construction because it requires that the results of the dynamic partitioning be stored in adjacent portions of the register. According to the plaintiff, the specifications of the media

processor patents disclose storing partitioned data in non-adjacent portions. The defendants contend that a person of ordinary skill in the art would understand that the data are stored in adjacent portions of registers. After considering the arguments of counsel, the court construes "storing partitioned data in registers" to mean "the results of the dynamic partitioning of the data stream are stored in registers."

**24. High bandwidth external interface**

The plaintiff argues that "high bandwidth external interface" means "an interface between the media processor and external sources of data capable of operating at or near a rate that maintains substantially peak operation of the media processor." The defendants urge that "high bandwidth external interface" means "an interface between the media processor and external sources of data that operates at or near the peak data throughput rate of the execution units [sic] of the media processor." The court construes "high bandwidth external interface" to mean "an interface between the media processor and external sources of data that is capable of operating at or near the peak data throughput rate of the execution unit of the media processor."

**25. A high bandwidth external interface operable to receive a plurality of data of various sizes from an external source and communicate the received data over the data path at a rate that maintains substantially peak operation of the media processor**

After considering the submissions of counsel, the court concludes that this phrase requires no additional construction.

**26. High bandwidth interface**

After considering the submissions of counsel, the court concludes that this phrase requires no additional construction.

**27. Substantially peak rates**

The court construes "substantially peak rates" to mean "simultaneous parallel processing using all or nearly all of the entire width of the data path."

**28. Data path**

The term "data path" is construed to mean "the buses and circuit elements that convey data."

**29. Bi-directional communication fabric**

The phrase "bi-directional communication fabric" means "an interprocessor communications network allowing communication in both directions." The specification suggests that the patentee used "network" and "fabric" interchangeably. *See* '840 patent, col. 6, ll. 16-19. At least one programmable media processor is provided within the communications network for receiving, processing, and transmitting the at least one stream of unified media data over the bi-directional communications fabric.

**30. Being capable of being represented by a defined bit width which is equal to said defined bit width of said operands**

The plaintiff proposes that this phrase means "able to be represented by a data field of the same size as the floating point operands." The defendants contend that the disputed phrase means "the bit width of the product of the permissible floating point operands must be no greater than the bit width of each of the operands." The plaintiff objects to the defendants' construction because of the limitation "no greater than the bit width of each of the operands." The claim language, the plaintiff argues, requires the capability of being represented by a bit width *equal to* the bit width of the operands. The defendants insist, however, that their "no greater than" limitation is entirely consistent with the claim language and is found in the specification of the '482 patent. After

considering the submissions of counsel, the court adopts the plaintiff's construction and construes "being capable of being represented by a defined bit width which is equal to said defined bit width of said operands" accordingly.

**31. Group floating point operations**

The court construes "group floating point operations" to mean "floating point operations applied to a group of partitioned operands."

**32. Dedicated memory**

The term "dedicated memory" appears in all of the claims of the '321 patent. In its reply brief, the plaintiff proposes that "dedicated memory" should be construed to mean "memory that is within the media processor that is accessible only through memory circuitry associated with the media processor." The defendants contend that under the plaintiff's construction, the memory is not dedicated because it is accessible by circuitry associated with the media processor and associated with another processor. Thus, the defendants insist that "dedicated memory" means "memory that is within the media processor that is accessible only through the media processor." Mindful that the claim language requires a "dedicated" memory, the court adopts the defendants' construction of "dedicated memory" and construes this term accordingly.

**33. Boolean . . . mathematical operation**

The court construes "Boolean . . . mathematical operation" as follows: "A Boolean operation is an operation that applies formal logic (for example, 'AND,' 'OR,' 'NOR,' etc.)."

## B. Disputed Terms of the '096 Patent

### 1. Throughput maximizing unit for processing said memory requests to the synchronous DRAM in response to scheduling which maximizes the use of data slots by the synchronous DRAM

The court first considers whether § 112 ¶ 6 applies. The plaintiff asserts that it does not and that the phrase "throughput maximizing unit for processing said memory requests . . ." means "an element of the controller that processes memory requests in response to scheduling constraints of the synchronous DRAM which maximizes the use of data slots." In their response brief, the defendants contend that "maximizing throughput of said memory requests . . ." is a means-plus-function limitation. The defendants argue that "claims 1 and 3 fail to recite any structure for processing memory requests to maximize the use of data slots, and claims 11,13, and 20 fail to recite any acts prescribing how to maximize the use of data slots." Defendants' Response Brief at 71. The absence of the word "means" raises a presumption that § 112, ¶ 6 does not apply. The court concludes that "throughput maximizing unit for processing said memory requests . . ." is not a means-plus-function limitation. The court therefore adopts the plaintiff's construction and construes "throughput maximizing unit for processing said memory requests" as an "element of the controller that processes memory requests in response to scheduling constraints of the synchronous DRAM which maximizes the use of data slots."

### 2. Throughput maximizing unit

The plaintiff proposes that the term "throughput maximizing unit" is "an element of the controller that processes memory requests in response to scheduling constraints of the synchronous DRAM." The defendants contend that the term "throughput maximizing unit" is a means-plus-function limitation. After considering the arguments of counsel, the court concludes that the term

"throughput maximizing unit" is not a means-plus-function limitation. Accordingly, the court construes "throughput maximizing unit" to mean "an element of the controller that processes memory requests in response to scheduling constraints of the synchronous DRAM, which maximizes throughput."

**3. Maximizing throughput of said memory requests to the synchronous DRAM so that use of the data slots by the synchronous DRAM is maximized**

The court adopts the plaintiff's construction of "maximizing throughput of said memory requests . . ." and construes this phrase to mean "scheduling memory requests to the synchronous DRAM to maximize throughput so that the use of data slots is maximized."

**4. Memory requests**

The term "memory requests" appears in all of the asserted claims of the '096 patent. The plaintiff proposes that "memory requests" are "requests from an external device, such as a processor, to a memory device." The defendants assert that "memory requests" are "requests from an external device such as a processor, to load data from or store data to the synchronous DRAM." The parties dispute whether "memory requests" must be directed to the synchronous DRAM. According to the defendants, "memory requests" are addressed only to the synchronous DRAM and not any other memory device. After considering the submissions of counsel, the court adopts the plaintiff's construction of "memory requests."

**5. Data slots**

The term "data slots" is recited in all of the asserted claims of the '096 patent. The plaintiff submits that "data slots" are "times during which data may be transferred to or from the SDRAM." The defendants propose that "data slots" are "SDRAM clock cycles for transferring data." The

plaintiff contends that the defendants propose "a highly specific construction of data slot related to the SDRAM clock cycle" that is not supported by or disclosed in the specification. However, the defendants argue that the '096 patent makes clear that the "data slots correspond to SDRAM clock cycles in Figs. 4(a -c) and does not disclose any other time period from which a data slot may be defined." Defendants' Sur-reply Brief at 20. After considering the submissions of counsel, the court construes the term "data slots" to mean "SDRAM clock cycles available for transferring data."

**6. Interfacing a processing device with a synchronous DRAM**

The plaintiff proposes that "interfacing a processing device with a synchronous DRAM" means "reading and writing to the synchronous DRAM by a processing device." The defendants urge that the disputed phrase means "translating memory requests into synchronous DRAM commands." At issue is whether "interfacing" requires translation. In its reply brief, the plaintiff argues that the defendants' proposed construction introduces a notion of translation, which is inconsistent with the ordinary meaning of the term "interfacing." On the other hand, the defendants contend that the disclosed controller receives memory requests and translates them into SDRAM commands. The court construes the phrase "interfacing a processing device with a synchronous DRAM" to mean "enabling reading and writing to the synchronous DRAM by a processing device."

**7. Sorting said memory requests based on their addresses**

The plaintiff urges that "sorting said memory requests based on their addresses" means "segregating memory requests into one or more groups based on their addresses." The defendants argue that the disputed phrase means "segregating memory requests into two or more groups according to their addresses." At issue is the number of groups into which "memory requests" can be segregated. The court adopts the plaintiff's construction of "sorting said memory requests based

on their addresses" and construes this phrase accordingly.

**8. Means for developing memory requests from the processing device**

This means-plus-function limitation appears in claim 10 of the '096 patent. The parties agree that the court need only construe the corresponding structure. The plaintiff contends that the corresponding structure is "bank sort unit 10 and equivalent structures." The defendants urge that the corresponding structure is "command update unit 210, bank qualification unit 220, and Tables 1-2." After considering the submissions of counsel, the court concludes that the corresponding structure consists of "bank sort unit 10 and equivalent structures."

SIGNED this 26th day of August, 2005.

T. John Ward

T. JOHN WARD
UNITED STATES DISTRICT JUDGE